

CFG Orion

***Release Notes***

**Version: ORION-19.01**

**Revision: A.0**

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CFG Orion 19.01 Release Notes

About This Document

This document lists the release notes for CFG Orion. Using CFG NocStudio, users can define NoC architectures, describe specifications and requirements, optimize the NoC design and finally generate the NoC IP files such as RTL, testbench, synthesis scripts, NoC IP documentation etc.

Audience

This document is intended for users of NocStudio:

* NoC Architects
* NoC Designers
* SoC Architects

Prerequisite

Before proceeding, you should generally understand:

* Basics of Network on Chip technology
* AMBA interconnect standards

Related Documents

The following documents can be used as a reference to this document.

* CFG NocStudio Orion User Manual
* CFG Orion IP Integration Spec

Customer Support

For technical support about this product and general information, contact CFG Support.

Revision History

|  |  |  |
| --- | --- | --- |
| Revision | Date | Updates |
| 0.0 | Jan 07, 2019 | Initial Version |
| A.0 | Feb 24, 2019 | Hot fixes:   1. NocStudio PerfSim when sim\_aid\_enable = yes 2. CSB address range 3. Address width correction for Synopsys PA   Enhancements:   1. UPF updates |

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# Deliverables

* CFG NocStudio Package contains N7 version of the tool supporting 16 layers and 256 bridges.
* NocStudio executable with interactive GUI.
* Verification checkers to be used in the DV environment.
* Sanity Test Bench.
* Documentation
  1. NocStudio User Manual: The User Guide describes how to set up a system using NocStudio and how to use it to generate CFG IP.
  2. IP Integration Spec: The Integration Manual describes how to integrate a configured network into a larger subsystem.
  3. Technical Reference Manual: The Technical Reference Manual describes how the functionality of the various NoC elements, the features and functions available, and how to dynamically change the functions using the programmer’s mode.

# Installation

## Licensing

NocStudio uses FlexLM based licensing hosted by Intel Central Licensing group using two dedicated license servers: one in Santa Clara and the other is located in Israel.

In addition to LM\_PROJECT, a linux environmental variable *NETSPD\_LICENSE\_FILE* shall be set as shown below in order to access the licenses. The LM\_PROJECT is essential for users not to check out the wrong combination of license features by accident.

setenv NETSPD\_LICENSE\_FILE [7010@netspeed01p.elic.intel.com:7010@netspeed02p.elic.intel.com](mailto:7010@netspeed01p.elic.intel.com:7010@netspeed02p.elic.intel.com)

For teams without LM\_PROJECT defined, a node-locked license file may be issued. Simply copy over the license file under NocStudio installation directory and renamed it as “license.dat”. If the license file resides in a separated folder, user may set environment variable *LM\_LICENSE\_FILE* before opening NocStudio.

## Deliverables / Tarball set

The CFG IPs and their configuration tool NocStudio have been packaged individually for maximum flexibility allowing mix and match. Each release is tagged with <yy><mm> where yy is the last 2 digits of the year and mm is the month in integer. As an example, release in Jan 2019 will be referenced as 1901 release. Un-tar all individual tarballs delivered as part of the tarball set using the command below.

linux% tar zxvf <tarball\_name>.tar.gz

Here is the complete tarball set in a given release: netspeed-<release>.<package>.tar.gz

**Tarball name Description Category**

netspeed-<release>.tar.gz NocStudio Base  
netspeed-<release>.iculibpkg.tar.gz Unicode ICU lib package Base

netspeed-<release>.cruxpkg.tar.gz Crux IP package (non-AMBA) NSIP IP

netspeed-<release>.orionpkg.tar.gz Orion IP package AMBA IP  
netspeed-<release>.geminipkg.tar.gz Gemini IP package AMBA IP  
netspeed-<release>.pegasuspkg.tar.gz Pegasus IP package AMBA IP

netspeed-<release>.ocppkg.tar.gz OCP support package Connectivity  
netspeed-<release>.daupkg.tar.gz Deadlock Avoidance Unit System

netspeed-<release>.syscpkg.tar.gz SysC (PA) support package Flow

netspeed-<release>.cpp48pkg.tar.gz C++ Modeling API support Flow  
package for gcc 4.8

netspeed-<release>.cpp61pkg.tar.gz C++ Modeling API support Flow  
package for gcc 6.1

**Note**:  
The release makes use of Qt libraries covered under LGPL: <http://qt-project.org/downloads>

# Feature Updates

## Configurable Slave Block

The current release allows users to add a Configurable Slave Block, which can be configured at design time with different kinds of on-chip storage like SRAM. Contact CFG Support for more details. This feature is preliminary and doesn’t have CSR support and Low-power support yet.

## Revised Register Names

In the current release, the register names have been revised to suit their functionality better. Refer Technical Reference Manual for details.

## UPF Support

The current release is equipped to support the UPF file generation, along with the CPF files. This feature is preliminary.

## Address Filtering With Reject Ranges

In the current release, address ranges can be specified with reject ranges to reject reads and/or writes for particular addresses, based on user requirements. Contact CFG Support for more details.

## Router Optimization

In the previous release, turn routers were present at each turn contributing to cost and latency. In the current release, NocStudio automatically removes these routers which were used for turn only. The pipeline modules in the RTL now consists of the port\_id in the name.

## APB Master

In this release, the user can add APB Master ports (*apbm*) to the NoC. This is a *BETA feature*.

Note that APB Slave ports are to be instantiated as *apb* itself and not *apbs*.

## SAI Support

CFG NocStudio now supports SAI (Secure Access Index) for firewall implementation. It can be configured in one of two ways, register-based or pin-based. However, the pin-based way is only for backward compatibility and will be deprecated in the upcoming release. Refer the Firewall section of the Technical Reference Manual for more information.

# EDA Tool Compatibility

* Cadence EDA tools were used for verification and synthesis of this product.
* Incisive RTL Simulator 15.22.012
* Genus RTL Synthesis 15.20-p004\_1
* HAL Linting tool 13.20.036
* Confirmal 15.10.120
* Compatibility testing has been done with VCS J-2014.12-SP3-3.
* For Platform Architrect, used GCC version is gcc-6.1.0a. (Backward compatible upto gcc-5.2.0-64)
* Please refer to IP Integration specification to enable/disable specific CFG checker in order to resolve or workaround any verification related issues, if any.

Contact your CFG or Synopsys support team for assistance.

# Errata

## Low-Power Support For LLC

There is currently no low-power support for configs with LLC.

# Changes to Commands and Properties

## Command Changes

|  |  |
| --- | --- |
| **Command Name** | **Comment** |
| add\_config\_slave\_block | Command to add a configurable slave block and its bridge |
| add\_csb\_storage | Command to add a storage component to a configurable slave block |
| del\_csb\_storage | Command to delete a storage component from a configurable slave block |
| list\_csb\_storage | Command to lists the storage components in one or more configurable slave blocks |
| csb\_storage\_prop | Command to set or view a named property of a storage component in the configurable slave block |

## Default Property Changes

|  |  |  |
| --- | --- | --- |
| **Property Name** | **Default Value** | **Comment** |
| axi4\_sai\_enable | no | This property on master bridges will expose additional AxSECGRP signals on the AXI AR and AW interfaces. |

## Mesh Property Changes

|  |  |  |
| --- | --- | --- |
| **Property Name** | **Default Value** | **Comment** |
| register\_based\_sai | no | If this property is set to yes, then register based SAI is enabled. If set to no, SAI related pins will be created on the Master and Slave bridges |

## Bridge Property Changes

|  |  |
| --- | --- |
| **Property Name** | **Comment** |
| axi4\_sai\_enable | This property on master bridges will expose additional AxSECGRP signals on the AXI AR and AW interfaces. |
| axi4m\_ar\_scgrp\_enable | This property determines which bits in the SAI access register are enabled |
| axi4m\_aw\_scgrp\_enable | This property determines which bits in the SAI access register are enabled |

## Host Property Changes

|  |  |  |
| --- | --- | --- |
| **Property Name** | **Default Value** | **Comment** |
| csb\_exclusive\_support | no | This property controls whether exclusive monitors are present in the configurable slave |
| csb\_data\_width | 64 | This property sets the data width of the configurable slave block |
| llc\_exclusive\_support | yes | This property controls whether exclusive monitors are present in LLC and ICCC. |

## Interface Property Changes

None

## Link Property Changes

None

## Router Property Changes

None

## VC Property Changes

None

## CSB Storage Property Changes

|  |  |  |
| --- | --- | --- |
| **Property Name** | **Default Value** | **Comment** |
| csb\_storage\_memory\_in\_width | 1 | This property sets the number of info bits needed as input to the CSB storage memory component |
| csb\_storage\_memory\_out\_width | 1 | This property sets the number of info bits needed as output to the CSB storage memory component |
| csb\_storage\_bandwidth\_delay | 1 | This value specifies the bandwidth of the directory |
| csb\_storage\_addr\_range | n/a | This property specifies a sub-address range for a storage component inside a configurable slave block |
| csb\_storage\_ecc\_enable | no | This property enables or disables ECC on the storage component in the configurable slave block. |
| csb\_storage\_num\_banks | 1 | This property sets the number of banks on the storge component inside the configurable slave block |
| csb\_storage\_latency | 1 | This property sets the latency which includes the latency for look-ups in the SRAM |
| csb\_storage\_secure\_access\_enable | no | This property enables or disables the need for secure accesses to the storage component in the configurable slave block. |
| csb\_storage\_type | Undefined | This property sets the type for the storage component in the configurable slave block. |
| csb\_storage\_capacity | 0 | This property sets the total capacity in KB for the storage component in the configurable slave block. |

# Hot fixes

## Corrected simulation crash issue when sim\_aid\_enable = yes

An issue related to NocStudio performance simulator crashes when sim\_aid\_enable = yes has been corrected. This allows users to mimic system serialization behavior while maintaining AXI ordering.

## Removed un-necessary address range checks on CSB

An un-necessary address range check on Configurable Slave Block with multiple storages has been relaxed. This allows users to configure continuguous and flexible addressing scheme for the system.

## SysC \*.tcl missing address width configuration

A missing address width configuration found in systemc/SC\_Model/\*.tcl has been corrected. For system with address width greater than 32, the user can now model full system address with minimal file modification before running Synopsys PA or PA-Ultra.

## UPF enhancements

A few corrections on UPF generation has been corrected. Please note that this feature remains preliminary in 1901\* release.

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